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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,552	11/14/2003	Duo Deng	130209.513	7977
500 7590 05/15/2007 SEED INTELLECTUAL PROPERTY LAW GROUP PLLC 701 FIFTH AVE SUITE 5400 SEATTLE, WA 98104			EXAMINER AMRANY, ADI	
			ART UNIT 2836	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/713,552	DENG ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Adi Amrany	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 13 February 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicants' arguments filed January 30, 2007 and applicants' Remarks filed February 13, 2007 (after the telephone interview) have been fully considered but they are not persuasive. During the telephone interview and again in the Remarks (2/13/07), applicants raised the possibility of interpreting the term "both" in claim 1 to mean "either of the two" or "always two." This conflicting interpretation requires a claim amendment to further define between the two definitions.

### ***Claim Objections***

2. Claim 24 is objected to because the phrase, "couple the DC power supply to the DC bus to supply from the DC power supply when a transient power source irregularity is detected," appears to be incorrect. There is no recitation of what is supplied/provided from the DC power supply. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janonis (US 5,612,580).

With respect to claim 19, Janonis discloses the apparatus necessary to complete the recited method. Janonis discloses a method for responding to electrical power

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source irregularities in an uninterruptible power supply system (figure 1, item 10; col. 2, lines 26-27), comprising:

providing an uninterruptible power supply system comprising an AC source converter (figure 1, item 32; col. 3, line 60 to col. 4, line 3) connectable to an AC power source (figure 1, item 12) and an AC load converter (figure 1, item 36) connectable to a load (figure 1, item 14), wherein the converters are interconnected by a DC bus (inherent, as discussed above);

interconnecting a rechargeable DC power supply (figure 1, item 28; col. 3, lines 5-24) to the DC bus (figure 1, connection between items 32-34-36, col. 3, line 60 to col. 4, line 3);

monitoring DC bus voltage on the DC bus (figure 1, items 12, 20; col. 2, lines 39-43; col. 3, lines 25-35);

establishing a first DC bus threshold voltage (col. 3, lines 36-45) indicative of a first power source irregularity and a second DC bus voltage threshold (col. 4, lines 9-15) indicative of a second and distinct power source irregularity, wherein the first threshold is greater than the second threshold;

comparing the DC bus voltage to the first and second thresholds (column 2, lines 39-43; col. 3, lines 43-45);

commuting electrical power from both the power source and from the DC power supply to the DC bus when the DC bus voltage is intermediate the first and second thresholds (figure 1, items 20, 22; col. 3, lines 46-59); and

conversely commuting electrical power only from the DC power supply to the DC bus when the DC bus voltage is less than the second threshold, and disabling the source converter (col. 4, lines 16-25).

Janonis does not expressly disclose monitoring a DC voltage on the DC bus, however, the examiner takes official notice that the voltage level of the power source can be sensed either as an AC voltage before the AC source converter, or as a DC voltage after the converter. Both AC and DC sensed voltages are directly related to the status of the AC input. The sensed voltages (AC and DC) are proportional to each other and to any changes/deviations in the level of the AC source voltage.

With respect to claim 20, Janonis further discloses establishing predetermined quality criteria for acceptable power source quality (col. 3, lines 43-45), monitoring power source voltage and current parameters on an input side of the source converter (col. 3, lines 29-31) and commuting electrical power only from the DC power supply to the DC bus and disabling the source converter when the power source voltage fails to meet the predetermined quality criteria indicative of a power source failure (col. 4, lines 9-15).

The Janonis UPS monitors the amplitude and frequency of in the input voltage to determine if it meets the quality criteria.

5. Claims 1-5, 8-14, 17-18, 21-23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janonis in view of Tassitino (US 5,633,539).

With respect to claims 1-5 and 8-9, the apparatus necessary to complete the recited methods is rejected, as provided below in the rejection of claims 10-14 and 17-18, respectively.

With respect to claim 10, Janonis discloses an apparatus for responding to electrical power source irregularities in an uninterruptible power supply system (figure 1, item 10; col. 2, lines 26-37) comprising a rechargeable DC power supply (figure 1, item 28; col. 3, lines 5-24) interconnected to a DC bus (figure 1, connection between items 32-34-36, col. 3, line 60 to col. 4, line 3), comprising:

means for monitoring (figure 1, items 12, 20; col. 2, lines 39-43; column 3, lines 25-35) DC bus voltage on the DC bus;

establishing means (col. 3, lines 36-45, col. 4, lines 9-15) for establishing a first DC bus voltage threshold indicative of a first power source irregularity and a second DC bus voltage threshold indicative of a second and distinct power source irregularity, wherein the first threshold is greater than the second threshold;

comparing means (col. 2, lines 39-43; col. 3, lines 43-45) for comparing the DC bus voltage to the first and second thresholds;

commuting means (figure 1, items 20, 22) for commuting electrical power from both the power source and from the DC power supply to the DC bus when the DC bus voltage is intermediate the first and second thresholds (col. 3, lines 46-59), and for conversely commuting electrical power only from the DC power

supply to the DC bus when the DC bus voltage is less than the second threshold and for disabling the source converter (col. 4, lines 16-25).

Janonis does not expressly disclose monitoring a DC voltage on the DC bus, however, the examiner takes official notice that the voltage level of the power source can be sensed either as an AC voltage before the AC source converter, or as a DC voltage after the converter.

Next, Janonis does not expressly disclose an uninterruptible power supply system comprising a three phase AC source converter connectable to a three phase AC power source and a three phase AC load converter connectable to a three phase load, wherein the converters are interconnected by a DC bus.

Tassitino discloses an uninterruptible power supply system (figure 1, item 100), comprising a three phase AC source converter (item 160) connectable to a three phase AC power source (item 110) and a three phase AC load converter (item 130) connectable to a three phase load (item 170), wherein the converters are interconnected by a DC bus (connection between items 160, 262, and 130). See also column 3, lines 17-34.

Janonis and Tassitino are analogous because they are from the same field of endeavor, namely uninterruptible power supplies that comprise backup DC power supplies with adjustable output voltages (Tassitino, col. 3, lines 35-67). At the time of the invention by applicants, it would have been obvious to a person of ordinary skill in the art to combine the uninterruptible power supply system comprising the off-line and on-line modes disclosed in Janonis with the 3 phase power supply, converters, and load

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disclosed in Tassitino in order to support a system that utilizes three-phase AC power, since it is a common power output delivered by utility companies.

With respect to claim 11, Tassitino further discloses the three-phase AC power source is a public power grid (col. 3, lines 17-20). The common method of transmitting power from a public utility to the customer is through a public power grid.

With respect to claim 12, Janonis further discloses the first power source irregularity is a transitory source instability (col. 3, lines 43-45, "sag or frequency deviation") and the second power source irregularity is a power source failure (col. 4, lines 9-15). The second threshold value in Janonis is lower than the first threshold value. Therefor, an input voltage that falls below the second threshold value may be considered more severe, and labeled a "power source failure." It is also inherent in Janonis that a power source failure that results in a full loss of supplied power to the UPS would be recognized as falling below the second threshold level, and would trigger the second on-line mode of operation.

With respect to claim 13, Janonis further discloses where the first power source irregularity is a transitory source instability and the second power source irregularity is a power source failure, as discussed above.

With respect to claim 14, Janonis further discloses:

grid failure establishing means (col. 3, lines 29-30) for establishing predetermined quality criteria for acceptable power source quality;



power source monitoring means (col. 3, lines 30-35) for monitoring source voltage and current parameters for each phase on an input side of the source converter;

and power source failure commuting means (col. 4, lines 17-19) for commuting electrical power only from the DC power supply to the DC bus and disabling the source converter when the source voltage fails to meet the predetermined quality criteria indicative of a power source failure.

As discussed above, the UPS in Janonis senses the input AC voltage before it is converted to DC, and it would be obvious to apply the three-phase AC UPS system disclosed in Tassitino to the AC UPS system disclosed in Janonis.

With respect to claim 17, Janonis further discloses a plurality of rechargeable DC power supplies (figure 1, item 28; col. 2, line 67 to col. 3, line 4) connected in parallel to each other and to the DC bus (figure 1, interconnection between items 32-34-36), and sequential DC power control means (col. 9, lines 8-19) for using power from each DC power supply sequentially when a power source irregularity is indicated. Janonis discloses that as more power is required to compensate for irregularities in the AC input voltage, more DC power supplies are activated.

Although Janonis does not expressly disclose that the rechargeable DC power supplies are connected in parallel to each other, it would have been obvious to combine each of the batteries in the Janonis battery array in parallel. The motivation for doing so would have been to increase the current supplied to the DC bus while maintaining a

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constant voltage. It is known in the art that voltage sources arranged in parallel act to add their respective current outputs while outputting a constant voltage level.

With respect to claim 18, Janonis further discloses the first threshold is 95-105 volts AC and the second threshold is 75 volts AC. As discussed above, it would be obvious that sensing the AC input voltage or converted DC input voltage would yield the same results regarding irregularities in the power source. Persons of ordinary skill in the art would extend or expand the operating threshold range to accommodate higher voltages for systems and loads having different design requirements. It has been decided that where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.

*In re Aller*, 220 F.2d 454, 456, 105 USPQ 223, 235 (CCPA 1955).

With respect to claim 21, Janonis discloses an apparatus for responding to electrical power source irregularities in an uninterruptible power supply system (figure 1, item 10; col. 2, lines 26-27) comprising a rechargeable DC power supply (figure 1, item 28; col. 3, lines 5-24) interconnected to a DC bus (figure 1, connection between items 32-34-36, col. 3, line 60 to col. 4, line 3), comprising:

an uninterruptible power supply system comprising a three phase AC source converter (figure 1, item 32; col. 3, line 60 to col. 4, line 3) connectable to a three phase AC power source (figure 1, item 12) and a three phase AC load converter (figure 1, item 36) connectable to a three phase load (figure 1, item 14), wherein the converters are interconnected by a DC bus;

a number of voltage sensors (figure 1, items 18, 30, 54; col. 2, lines 39-47) coupled to sense DC bus voltage on the DC bus;

a controller (figure 1, item 20; col. 3, lines 29-35) configured to compare the DC bus voltage to a first DC bus voltage threshold (column 3 lines 36-45) indicative of a first power source irregularity and a second DC bus voltage threshold (col. 4, lines 9-15) indicative of a second and distinct power source irregularity, wherein the first threshold is greater than the second threshold (col. 3, lines 39-41); and further configured to provide control signals to at least one of the three phase AC source converter and the three phase load converter to *commute* electrical power from both the power source and from the DC power supply to the DC bus when the DC bus voltage is intermediate the first and second thresholds (col. 3, lines 46-59), and for conversely commuting electrical power only from the DC power supply to the DC bus when the DC bus voltage is less than the second threshold and for disabling the source converter (col. 4, lines 13-25).

Official notice is given that the voltage level of the power source can be sensed either as an AC voltage before the AC source converter, or as a DC voltage after the converter, as discussed above. Tassitino discloses the three phase AC source voltage, as discussed above.

With respect to claim 22, Janonis further discloses the first power source irregularity is a transitory source instability (col. 3, lines 43-45) and the second power source irregularity is a power source failure (column 4, lines 9-15).

With respect to claim 23, Janonis further discloses a number of power source voltage sensors (figure 1, item 18; col. 2, lines 39-43) coupled to sense a source voltage for each phase on an input side of the source converter, and a number of power source current sensors coupled to sense a source current for each phase the input side of the source converter (figure 1, item 18), wherein the controller is further configured to *commute* electrical power only from the DC power supply to the DC bus and disabling the source converter when the source voltage fails to meet a predetermined quality indicative of a power source failure (col. 4, lines 9-15).

Janonis discloses a line condition sensor (item 18) for measuring diagnostic information on the power source line. While Janonis does not expressly disclose that the condition sensor is either a voltage or current sensor, it would have been obvious to a person of ordinary skill in the art that the condition sensor meets the requirements of both. In the recited apparatus, the voltage and current sensors are interchangeable. They perform the same function and yield proportional results regarding the quality of the power source.

Further, Janonis discloses a condition sensor, but does not expressly disclose that the condition sensor comprises *a number* of voltage and/or current sensors. It would have been obvious to one having ordinary skill at the time the invention was made to place a plurality of voltage and/or current sensors at the input side of the source converter, and to place a voltage and/or current sensor to measure each AC phase line, because the mere duplication of the essential working parts of a device

involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (1977).

With respect to claim 25, Janonis further discloses a plurality of rechargeable DC power supplies (figure 1, item 28; col. 2, line 67 to col. 3, line 4) connected in parallel to each other and to the DC bus (figure 1, connection between items 32-34-36), wherein the controller is configured to use power from each DC power supply sequentially when a power source irregularity is indicated. The arrangement of the rechargeable DC power supplies in parallel is obvious, as discussed above.

6. Claims 6-7, 15-16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janonis, in view of Tassitino and Faria (US 6,295,215).

With respect to claims 6-7, Janonis and Tassitino disclose the apparatus necessary to complete the recited method, as discussed below in the rejections of claims 15 and 16, respectively.

With respect to claim 15, Janonis and Tassitino do not expressly disclose instantaneous monitoring means for monitoring instantaneous load voltage and current parameters for each phase on an output side of the load converter, load power calculating means for calculating a load power demand value from the instantaneous parameters, transient power supplying means for supplying power to the DC bus from the DC power supply when a transient power source irregularity is indicated, and command signal generating means for generating a command signal to the DC power supply indicative of additional current needed by the load to supplant power lost from the AC power source due to the irregularity.

Faria discloses an uninterruptible power supply apparatus comprising:

instantaneous monitoring means (figure 3, item 325, 324; col. 6, lines 23-27) for monitoring instantaneous load voltage and current parameters for each phase on an output side of the load converter;

load power calculating means (figure 3, item 325, 322; col. 6, lines 27-3) for calculating a load power demand value from the instantaneous parameters;

transient power supplying means (col. 6, lines 11-15) for supplying power to the DC bus from the DC power supply when a transient power source irregularity is indicated;

and command signal generating means (col. 6, lines 37-45) for generating a command signal to the DC power supply indicative of additional current needed by the load to supplant power lost from the AC power source due to the irregularity.

Faria discloses an "economy mode", in which both the AC power source and DC power supply contribute to the output voltage. It is obvious that any sag or drop in the voltage level of the AC power source will be supported by an increase in the voltage output of the DC power supply. Therefore, the "economy mode" compensate disclosed in Faria comprises a command signal generating means.

Janonis, Tassitino, and Faria are analogous because they are from the same field of endeavor, namely uninterruptible power supplies that comprise backup DC power supplies with adjustable output voltages. At the time of the invention by applicants, it would have been obvious to a person of ordinary skill in the art to combine

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the three-phase AC uninterruptible power supply system comprising the off-line and on-line modes disclosed in Janonis and Tassitino with load converter output current and voltage sensing disclosed in Faria in order to detect a sag, drop, or irregularity in input voltage. The AC input voltage may be calculated based on the sensed load voltage minus the DC power supply voltage, which is known.

With respect to claim 16, Faria, as discussed above, discloses the apparatus comprises instantaneous monitoring means for monitoring instantaneous load voltage and current parameters for each phase on an output side of the load converter, load power calculating means for calculating a load power demand value from the instantaneous parameters, transient power supplying means for supplying power to the DC bus from the DC power supply when a transient power source irregularity is indicated, and command signal generating means for generating a command signal to the DC power supply indicative of additional current needed by the load to supplant power lost from the AC power source due to the irregularity.

With respect to claim 24, Faria discloses an uninterruptible power supply apparatus comprising:

- a number of voltage sensors (figure 3, item 325, 324; col. 6, lines 23-27) coupled to instantaneously sense load voltage for each phase of an output side of the load converter;

- a number of current sensors (figure 3, item 325, 324) coupled to instantaneously sense load current for each phase on an output side of the load converter, wherein the controller is further configured to calculate a load power

demand value (figure 3, item 325, 322; col. 6, lines 27-3) from the instantaneous load voltage and the instantaneous load current;

a transient power switch (col. 6, lines 11-15) selectively operable to couple the DC power supply to the DC bus to supply from the DC power supply when a transient power source irregularity is indicated; wherein the controller is further configured to generate a command signal (col. 6, lines 37-45) to the DC power supply indicative of additional current needed by the load to supplant power lost from the AC power source due to the irregularity.

The plurality of voltage/current sensors, coupled to sense the load for each phase of the output side of the load converter, is obvious in view of the duplication of parts, as discussed in the rejection of claim 23. Further, the interchangeability of voltage and current sensors would be obvious to a person skilled in the art, as discussed above.

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of



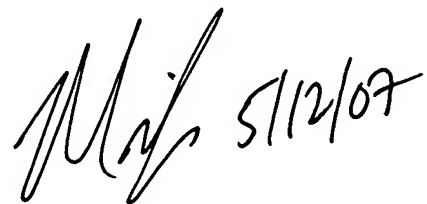
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA



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